Digital Charge Balance Controller With an Auxiliary Circuit for Improved Unloading Transient Performance of Buck Converters

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***Abstract*—In this paper, a digital charge balance controller is presented which is capable of controlling a buck converter and an auxiliary circuit to achieve an excellent unloading transient response. The auxiliary circuit significantly reduces the voltage overshoot caused by an unloading transient, while the digital charge balance controller reduces the settling time of the converter. The controller is capable of implementing load-line regulation and yields a smooth transition from one loading condition to another. Simulation and experimental verification is performed and demonstrates significant transient improvement over previously proposed solutions.**

***Index Terms*—DC-DC converters, load transient response, nonlinear control.**

I. Introduction

As the capabilities of high-performance digital devices continue to exponentially expand, the demand on the power electronics industry to supply such devices becomes increasingly complex. Load transients of digital devices are becoming larger, while physical real-estate constraints are becoming tighter preventing the tried-and-true method of adding capacitors to improve the transient performance of buck converters. Thus, extensive research has been conducted developing controllers which improve the transient performance of buck converters to their physical limits.

In [1]–[11], controllers have been presented which utilize second-order sliding surfaces, precalculated switching time intervals, or capacitor charge balance methodologies to reduce the voltage deviation and settling time of a buck converter, undergoing a load transient, to its virtually optimal level.

However, it is demonstrated in [1] and [2] that for low duty cycle conversion applications (e.g., 12 $V_{DC} \rightarrow 1.5\ V_{DC}$), the optimal voltage overshoot caused by a unloading transient may be more than five times as large as the corresponding voltage undershoot caused by a loading current step of equal magnitude, as illustrated in Fig. 1. Therefore, to adhere to voltage specifications, capacitor selection must be based on the larger voltage overshoot condition.

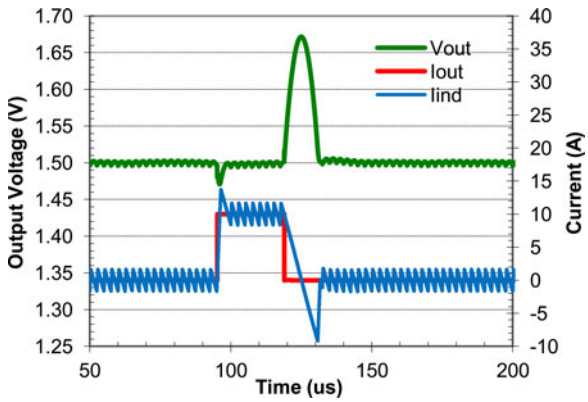

Fig. 1. Asymmetrical transient response to positive/negative load current step change (charge balance controller response).

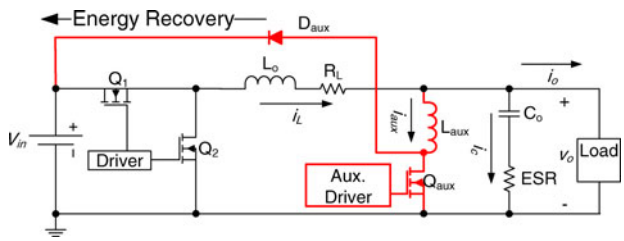

Fig. 2. Implementation of high-frequency auxiliary circuit [12].

Thus, in [12]–[22], various auxiliary circuits for the buck converter have been proposed to improve the transient performance of a converter undergoing high-to-low load current changes. Methods include temporarily inversing the converter's input voltage [13], temporarily disconnecting the inductor from the load [16], or diverting a portion of the inductor current to the input of the buck converter through a separate switching circuit [12], [21], [23].

For example, the unloading transient response is improved in [12] and [23] by utilizing a high-frequency switching auxiliary circuit (presented in [12] and illustrated in Fig. 2), which rapidly transfers current from the output of the buck converter to its input.

The control method presented in [12] diverts a predetermined fraction of the unloading transient magnitude to the input of the

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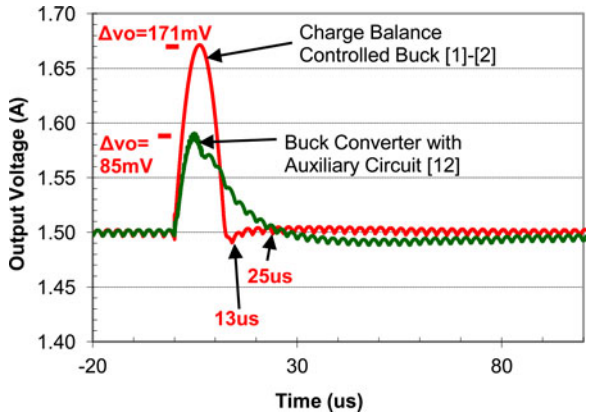

Fig. 3. Charge balance control response [1], [2] versus auxiliary circuit response [12].

buck converter. It employs a peak-current mode constant off-time controller in order to tightly regulate the auxiliary current.

While such methods do improve the unloading transient performance of the buck converter, there has been no attempt to simultaneously reduce the voltage overshoot and minimize the settling time through control methods such as those presented in [1]–[11]. Note: an exception to the previous statement is the work of Wen and Trescases [23]; provided that the control method in [23] can calculate the proper open-loop auxiliary duty cycle without error (i.e., the main/auxiliary inductor value tolerances are calibrated and the input voltage/output voltage remains relatively constant), the settling time is minimized.

The control method presented in [23] attempts to divert all excess inductor current to the input of the buck converter during a transient event. The controller presented in [23] controls the auxiliary circuit through an open-loop fixed duty cycle which is calculated based on the measured output voltage and estimated input voltage.

While work presented in [23] demonstrates a superior unloading transient over that in [12], drawbacks in [23] include the following:

1) higher saturation current limits required for the auxiliary inductor;
2) larger auxiliary circuit conduction losses due to higher RMS currents;
3) loose control of auxiliary current due to open-loop operation of the auxiliary circuit; sensitive to input/output voltage fluctuations;
4) series resistance added to output capacitor required to measure capacitor current, which is not practical in most applications.

Furthermore, previously proposed methods do not address applications in which load-line regulation is required.

Fig. 3 shows a simulated comparison of the unloading transient response of the nonlinear charge balance controller (presented in [1] and [2]) versus the auxiliary circuit and control method (presented in [12]). It is shown in Fig. 3 that while the addition of the aforementioned auxiliary circuit significantly reduces the voltage overshoot caused by an unloading transient, the settling time of the charge balance controller is far superior.

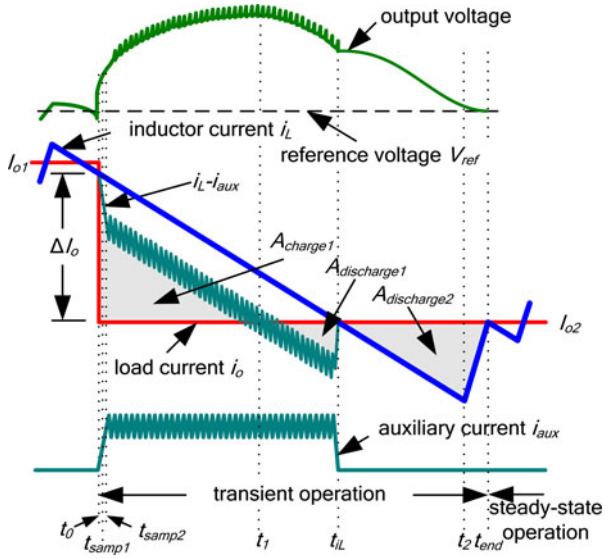

Fig. 4. Proposed controller reaction to an unloading transient (w/o load-line regulation).

In this paper, a digital charge balance controller is proposed which combines the auxiliary circuit, presented in [12] and illustrated in Fig. 2, with the control methodology presented in [1] and [2] to yield a converter with superior unloading transient performance. The proposed method actively reduces the output voltage overshoot caused by an unloading transient while minimizing the settling time to virtually optimal levels. To perform capacitor charge balancing, the proposed controller observes the output voltage during the beginning of the transient event and calculates the output capacitor current using a digital approximation method. Therefore, unlike [23], a series resistor is not required to measure the capacitor current.

Since the detailed implementation of the auxiliary circuit is covered extensively in [12], this paper will focus primarily on the proposed charge balance controller's ability to integrate with the controlled auxiliary circuit.

Section II will outline the concept of operation of the proposed controller. Section III demonstrates how capacitor charge balance integral regions can be calculated using a digital accumulator while driving a controlled auxiliary current. Section IV outlines the step-by-step operation for the proposed controller. Sections V and VI provide simulation and experimental results, respectively. Section VII provides a brief conclusion.

II. Concept of Operation

The controller's transient response will be described without and with load-line regulation.

A. Operation Without Load-Line Regulation

Fig. 4 illustrates the proposed controller's reaction to a rapid unloading transient without load-line regulation.

The high-level operation can be described in five steps.

1) The converter is controlled by a linear voltage-mode control scheme during steady-state conditions.

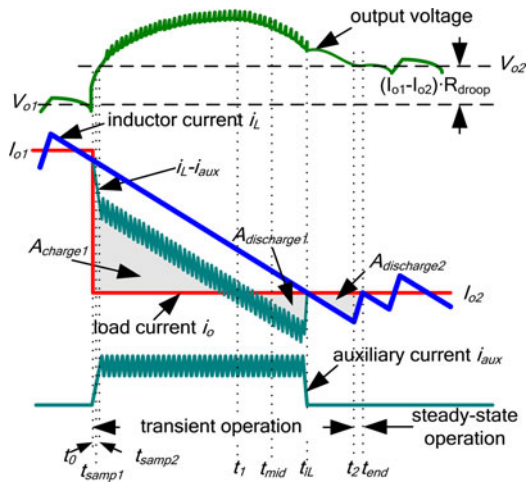

Fig. 5. Controller reaction to an unloading transient with load-line regulation (Case #1).

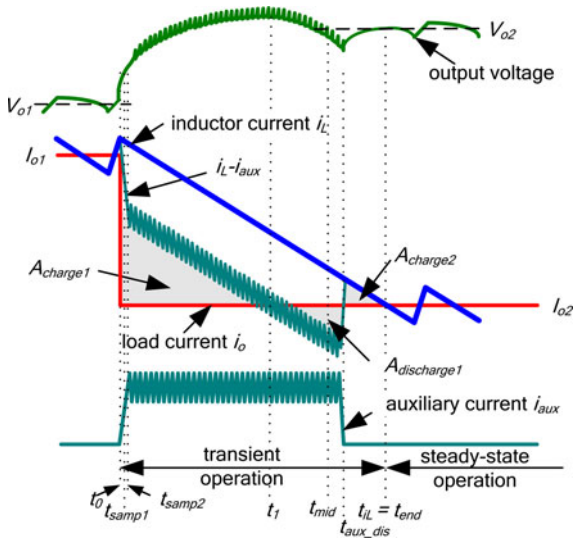

Fig. 6. Controller reaction to an unloading transient with load-line regulation (Case #2).

2) Immediately following an unloading transient, the controller will set the buck converter's pulsewidth modulation (PWM) signal low and set the auxiliary circuit's PWM signal high.
3) The controller will estimate the magnitude of the unloading transient $|\Delta I_o|$ and set the peak auxiliary current to an appropriate level based on $|\Delta I_o|$. At this point, the auxiliary circuit will begin switching operation (using peak-current, constant off-time control), transferring current from the buck converter's output to its input.
4) At the moment that the inductor current i_L first equals the new load current I_{o2} (at t_{iL}), the auxiliary circuit is deactivated. However, the buck converter's PWM signal will continue to remain low.
5) The buck converter's PWM signal will be set high at t_2 causing the inductor current to increase toward I_{o2}. t_2 should be such that the net capacitor charge is equal to zero at the exact moment that the inductor current equals the new load current for a second time. In other words, referring to Fig. 4, $A_{\text{charge1}} = A_{\text{discharge1}} + A_{\text{discharge2}}$ when $i_L = I_{o2}$ at t_{end}. This will ensure that the output voltage and the inductor current equal their respective steady-state values simultaneously at t_{end}.

B. Operation With Load-Line Regulation

Two cases must be addressed when charge balance control, the auxiliary circuit, and load-line regulation are employed. The occurrence of the two cases depends on the converter parameter selection and the magnitude of the transient load current step.

1) Case #1 ($v_o > V_{o2}$ When $i_L = I_{o2}$): As illustrated in Fig. 5, Case #1 occurs when the output voltage v_o of the converter is greater than the new steady-state output voltage V_{o2} at the moment that the inductor current i_L equals the new load current I_{o2}.

As shown, at the moment that i_L first equals I_{o2} ($t = t_{iL}$), the auxiliary circuit is deactivated and the auxiliary current decreases to zero; however, additional charge must be removed from the capacitor such that the output voltage can be decreased to its new steady-voltage V_{o2}. Therefore, the PWM control signal will remain low until t_2. t_2 is such that the charge balance equation is true

$$A_{\text{charge1}} - A_{\text{discharge1}} - A_{\text{discharge2}} = \int_{t_0}^{t_1} (i_L - i_{\text{aux}} - i_o)dt - \int_{t_1}^{t_{iL}} (i_o - i_{\text{aux}} - i_L)dt - \int_{t_{iL}}^{t_2} (i_o - i_L)dt = (I_{o1} - I_{o2}) \cdot R_{\text{droop}} \cdot C_o \quad (1)$$

where A_{charge1}, $A_{\text{discharge1}}$, and $A_{\text{discharge2}}$ are the capacitor current integral areas shown in Fig. 5.

Referring to (1), it is noted that C_o is required to solve the right-hand side of the equation. The right-hand side of (1) represents the positive net change in capacitor charge required due to load-line regulation. The final voltage error (at t_{end}) due to C_o tolerance is proportional to the C_o multiplied by R_{droop}, multiplied by the load step magnitude. It is important to note that if $R_{\text{droop}} = 0$ (i.e., load-line regulation is not employed), the C_o tolerance does not affect the charge balance equations.

This section provides a brief overview of the operation of the controller. The detailed step-by-step operation of the controller will be presented in Section IV.

2) Case #2 ($v_o = V_{o2}$ Before $i_L = I_{o2}$): Case #2 is shown in Fig. 6. As shown, during Case #2, the output voltage v_o equals its new steady-state voltage V_{o2} before i_L equals I_{o2}. In this case, the auxiliary circuit will be deactivated *prior* to i_L equalling I_{o2} (at $t_{\text{aux\_dis}}$). $t_{\text{aux\_dis}}$ will be such that the following equation is satisfied:

$$A_{\text{charge1}} - A_{\text{discharge1}} - A_{\text{charge2}} = \int_{t_0}^{t_1} (i_L - i_{\text{aux}} - i_o)dt - \int_{t_1}^{t_{\text{aux\_dis}}} (i_o - i_{\text{aux}} - i_L)dt + \int_{t_{\text{aux\_dis}}}^{t_{\text{end}}} (i_L - i_o)dt = (I_{o1} - I_{o2}) \cdot R_{\text{droop}} \cdot C_o. \quad (2)$$

The buck converter's PWM signal will be held low until the inductor current equals the new load current (at t_{iL}). At this point, the linear controller will retain control. The controller is capable of automatically detecting the aforementioned cases. The detection method will be described in detail in Section IV.

III. Mathematical Analysis of Charge Balance Controller With Auxiliary Circuit

This section will derive the charge balance equations necessary to implement digital charge balance control such that a buck converter, with the proposed auxiliary circuit, will recover from an unloading transient with minimal settling time. The charge balance equations are presented at first without load-line regulation and then with load-line regulation.

A. Without Load-Line Regulation

Referring to Fig. 4, it is noted that there is one positive integral area of capacitor current A_{charge1} and two negative integral areas of capacitor current $A_{\text{discharge1}}$ and $A_{\text{discharge2}}$. The capacitor charge area A_{charge1} is derived as follows:

$$A_{\text{charge1}} = \iint_{t_0}^{t_1} m_2 dtdt \tag{3}$$

where m_2 is the falling slew rate of the inductor current i_L ($m_2 \approx V_o/L_o$) and t_1 represents the first moment that the capacitor current i_c equals zero (i.e., when $i_L - I_{\text{aux\_avg}} = I_{o2}$).

It is noted that the inductor current slew rate is assumed independent of the output current. In other words, the dc resistance (DCR) of the inductor has been neglected. For low-voltage high-current applications, the inductor DCR is typically very low and causes an insignificant effect on the inductor current slew rate.

Referring to Fig. 4, it is shown that the auxiliary circuit is deactivated when the inductor current equals the new load current (at t_{iL}). It is assumed that when the auxiliary circuit is deactivated, the auxiliary current i_{aux} decreases to zero in negligible time. This is a fair assumption since the falling i_{aux} slew rate is much faster than the falling i_L slew rate. For the charge balance equations, the ripple of the auxiliary current is neglected since the high-frequency auxiliary switching causes the ripple's effect to be neutralized.

With the aforementioned assumptions, $A_{\text{discharge1}}$ is calculated as follows:

$$A_{\text{discharge1}} = \iint_{t_1}^{t_{iL}} m_2 dtdt. \tag{4}$$

Through geometric observation and simplification, $A_{\text{discharge2}}$ is expressed as follows:

$$A_{\text{discharge2}} = \iint_{t_{iL}}^{t_2} \frac{m_1 \cdot m_2 + m_2^2}{m_1} dtdt \tag{5}$$

where m_1 is the rising slew rate of the inductor current i_L ($m_1 \approx (V_{\text{in}} - V_o)/L_o$). In order to ensure that v_o and i_L equal their respective steady-state values simultaneously, the net capacitor charge over the transient period must equal zero:

$$A_{\text{charge1}} - A_{\text{discharge1}} - A_{\text{discharge2}} = 0$$

$$\iint_{t_0}^{t_1} m_2 dtdt - \iint_{t_1}^{t_{iL}} m_2 dtdt - \iint_{t_{iL}}^{t_2} \frac{m_1 \cdot m_2 + m_2^2}{m_1} dtdt = 0. \tag{6}$$

By dividing both sides of (6) by the constant m_2, substituting the known values for m_1 and m_2, multiplying both sides by $(V_{\text{in}} - V_o)$, and simplifying, we obtain

$$(V_{\text{in}} - V_o) \cdot \iint_{t_0}^{t_1} dt\, dt - (V_{\text{in}} - V_o) \cdot \iint_{t_1}^{t_{iL}} dt\, dt - V_{\text{in}} \cdot \iint_{t_{iL}}^{t_2} dt\, dt = 0. \tag{7}$$

Therefore, by using (7), it is possible to determine the moment that the buck converter's PWM control signal should be set high (at t_2), by the use of two accumulators, connected in series. The waveforms of the double accumulator are shown in Fig. 7.

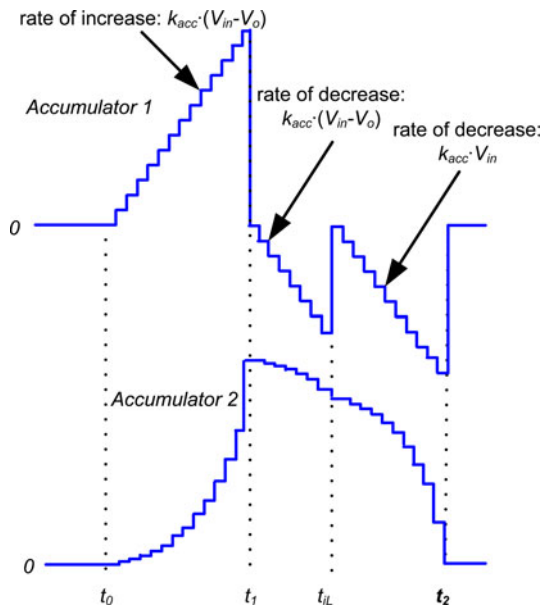

Fig. 7. Digital double accumulator to determine t_2 without load-line regulation.

The constant k_{acc} represents the gain of the digital accumulators and is dependent on the system clock frequency. As shown, when the output of *accumulator 2* returns to zero, t_2 is determined and the buck converter's PWM signal is set high. This control strategy is suitable when load-line regulation is not employed; however, it must be modified when load-line regulation is employed.

B. With Load-Line Regulation

This section will be divided into Case #1 and Case #2, as previously described in Section II.

1) Case #1 ($v_o > V_{o2}$ When $i_L = I_{o2}$): The capacitor charge regions for Case #1 are illustrated in Fig. 8. As shown, a time instant t_{mid} has been identified in Fig. 8. t_{mid} bisects time instants

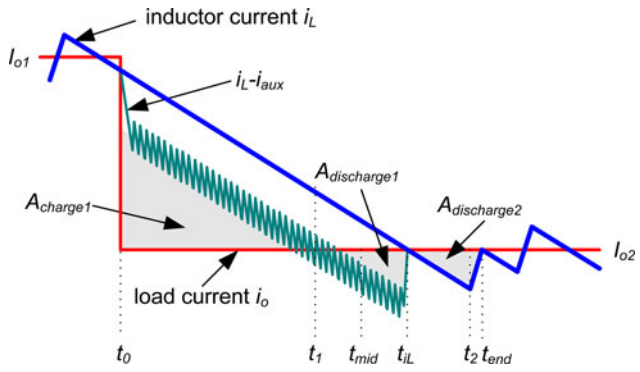

Fig. 8. Capacitor charge regions for load-line regulation (Case #1).

t_1 and t_{iL} and will be used in the charge balance calculation. As will be discussed, $t_{\rm mid}$ is significant because it is the earliest possible moment that the controller must make a decision between Case #1 action and Case #2 action. $t_{\rm mid}$ occurs when the following equation is true:

$$i_L - I_{o2} = \frac{1}{2} \cdot I_{\rm aux_{avg}}, \quad \text{when } t = t_{\rm mid}. \tag{8}$$

The method of detecting $t_{\rm mid}$ will be discussed in Section IV.

The charge balance equation can be obtained by modifying (6) as

$$\begin{aligned} A_{\rm charge1} - A_{\rm discharge1} - A_{\rm discharge2} &= (I_{o1} - I_{o2}) \cdot R_{\rm droop} \cdot C_o \\ \iint_{t_0}^{t_1} m_2 dt dt - \iint_{t_1}^{t_{iL}} m_2 dt dt - \iint_{t_{iL}}^{t_2} \frac{m_1 \cdot m_2 + m_2^2}{m_1} dt dt &= (I_{o1} - I_{o2}) \cdot R_{\rm droop} \cdot C_o. \end{aligned} \tag{9}$$

The right-hand side of (9) represents the required capacitor charge offset to implement load-line regulation. By integrating m_2 for the time interval from the beginning of the transient t_0 to the capacitor current zero-crossover point t_1, the change in load current $(I_{o1} - I_{o2})$ can be estimated, as shown in the right-hand side of the following equation:

$$\iint_{t_0}^{t_1} m_2 dt dt - \iint_{t_1}^{t_{iL}} m_2 dt dt - \iint_{t_{iL}}^{t_2} \frac{m_1 \cdot m_2 + m_2^2}{m_1} dt dt = R_{\rm droop} \cdot C_o \cdot \int_{t_0}^{t_1} m_2 dt. \tag{10}$$

It is assumed that the load current step magnitude is large as compared to the magnitude of the steady-state capacitor ripple current.

Since m_1 and m_2 are assumed constant, the terms can be moved outside the integral. Both sides of (10) are then divided by m_2 to obtain

$$\iint_{t_0}^{t_1} dt dt - \iint_{t_1}^{t_{iL}} dt dt - \iint_{t_{iL}}^{t_2} \frac{m_1 + m_2}{m_1} dt dt = R_{\rm droop} \cdot C_o \cdot \int_{t_0}^{t_1} dt. \tag{11}$$

The rising $[m_1 = (V_{\rm in} - V_o)/L_o]$ and falling $(m_2 = V_o/L_o)$ inductor current slew rates are substituted into (11) and the equation is simplified to obtain

$$\begin{aligned} (V_{\rm in} - V_o) \cdot \iint_{t_0}^{t_1} dt\, dt - (V_{\rm in} - V_o) \cdot \iint_{t_1}^{t_{iL}} dt\, dt - V_{\rm in} \\ \cdot \iint_{t_{iL}}^{t_2} dt\, dt = (V_{\rm in} - V_o) \cdot R_{\rm droop} \cdot C_o \cdot \int_{t_0}^{t_{iL}} dt. \end{aligned} \tag{12}$$

In these calculations, it will be assumed that the output voltage is equal to the initial output voltage at the beginning of the transient (i.e., $V_o = V_{o1}$). As expressed, the output of an additional accumulator (the *load-line accumulator*) is compared with the output of the double accumulator to determine t_2.

Since $t_{\rm mid}$ bisects time instances t_1 and t_{iL}, by definition, the integration of time from t_0 to t_{iL} can be modified as

$$\begin{aligned} \int_{t_0}^{t_{iL}} dt &= \int_{t_0}^{t_1} dt + \int_{t_1}^{t_{iL}} dt \\ &= \int_{t_0}^{t_1} dt + \int_{t_1}^{t_{\rm mid}} dt + \int_{t_{\rm mid}}^{t_{iL}} dt \\ &= \int_{t_0}^{t_1} dt + 2 \cdot \int_{t_1}^{t_{\rm mid}} dt. \end{aligned} \tag{13}$$

By substituting (13) into (9), the charge balance equation for load-line regulation (Case #1) is derived as follows:

$$\begin{aligned} (V_{\rm in} - V_o) \cdot \iint_{t_0}^{t_1} dt\, dt - (V_{\rm in} - V_o) \cdot \iint_{t_1}^{t_{iL}} dt\, dt \\ - V_{\rm in} \cdot \iint_{t_{iL}}^{t_2} dt\, dt \\ = (V_{\rm in} - V_o) \cdot R_{\rm droop} \cdot C_o \cdot \left(\int_{t_0}^{t_1} dt + 2 \cdot \int_{t_1}^{t_{\rm mid}} dt \right). \end{aligned} \tag{14}$$

Thus, t_2 can be determined by using the aforementioned double accumulator [left-hand side of (14)] and comparing its output with the output of a single accumulator [right-hand side of (14)]. Fig. 9 illustrates the operation of a digital double accumulator to calculate the switching instant t_2.

2) Case #2 ($v_o = V_{o2}$ Before $i_L = I_{o2}$): The capacitor charge regions for Case #2 are closely examined in Fig. 10. It is shown that, for Case #2, the moment the auxiliary circuit is deactivated $t_{\rm aux\_dis}$ occurs before t_{iL} to allow charge area $A_{\rm charge2}$ to charge the output capacitor.

If the auxiliary circuit were deactivated at $t_{\rm mid}$, the capacitor current $(i_L - I_{o2})$ would equal $I_{o2} + I_{\rm aux\_avg}$, which can also be expressed in terms of the falling inductor slew rate as

$$i_L(t_{\rm mid}) - I_{o2} = \int_{t_1}^{t_{\rm mid}} m_2 dt. \tag{15}$$

Following $t_{\rm mid}$, the potential charge area $A_{\rm charge2}$ begins to decrease as the inductor current approaches the new load current

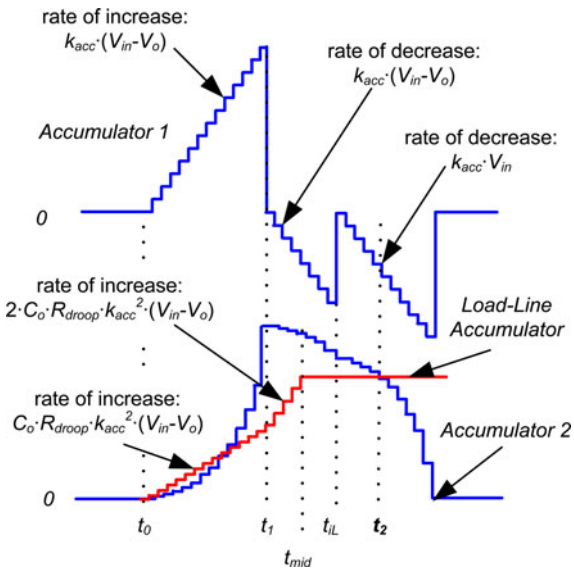

Fig. 9. Digital double accumulator to determine t_2 with load-line regulation (Case #1).

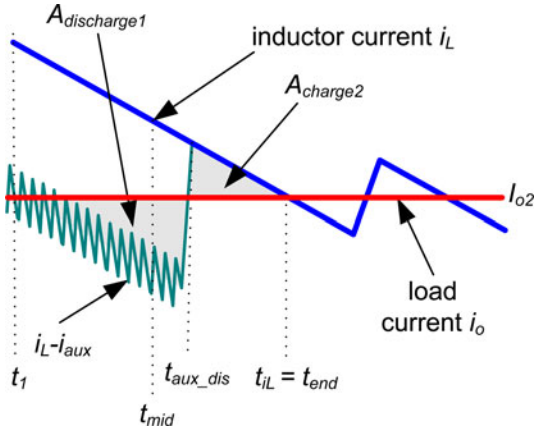

Fig. 10. Capacitor charge areas for Case #2.

at a slew rate of m_2. Thus, A_{charge2} is expressed as follows:

$$A_{\text{charge2}} = A_{\text{discharge1}} - \int_{t_{\text{mid}}}^{t_{\text{aux\_dis}}} \left(i_L(t_{\text{mid}}) - I_{o2} - m_2 \cdot \int_{t_{\text{mid}}}^{t_{\text{aux\_dis}}} dt \right) d\tau. \quad (16)$$

By substituting (3), (4), (13), and (16) into (2), the charge balance equation for Case #2 load-line regulation is expressed as follows:

$$\iint_{t_0}^{t_1} m_2\, dtdt - \iint_{t_1}^{t_{\text{aux\_dis}}} m_2\, dtdt + \iint_{t_1}^{t_{\text{mid}}} m_2\, dt\, dt - \int_{t_{\text{mid}}}^{t_{\text{aux\_dis}}} \left(\int_{t_1}^{t_{\text{mid}}} m_2 dt - \int_{\text{mid}}^{t_{\text{aux\_dis}}} m_2 dt \right) d\tau = R_{\text{droop}} \cdot C_o \left(\int_{t_0}^{t_1} m_2 dt + 2 \cdot \int_{t_1}^{t_{\text{mid}}} m_2 dt \right). \quad (17)$$

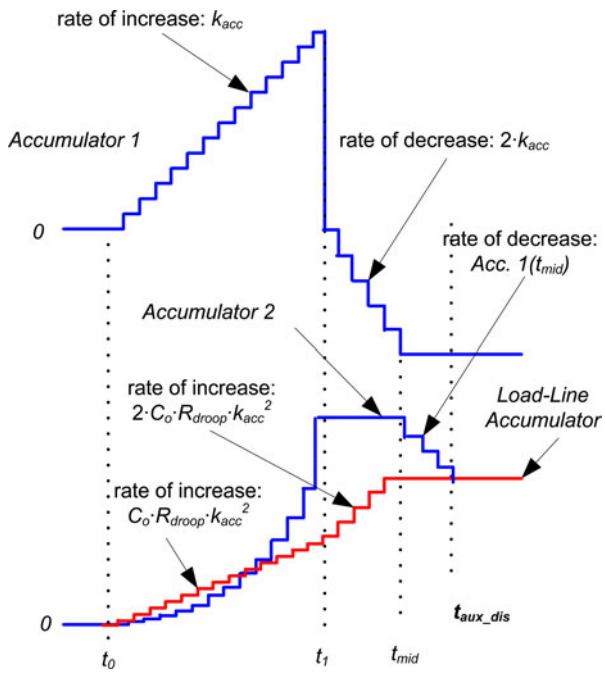

Fig. 11. Digital double accumulator to determine $t_{\text{aux\_dis}}$ with load-line regulation (Case #2).

By collecting like terms, (17) is simplified as

$$\iint_{t_0}^{t_1} dtdt - \int_{t_{\text{mid}}}^{t_{\text{aux\_dis}}} \left(2 \cdot \int_{t_1}^{t_{\text{mid}}} dt \right) dt = R_{\text{droop}} \cdot C_o \left(\int_{t_0}^{t_1} dt + 2 \cdot \int_{t_1}^{t_{\text{mid}}} dt \right). \quad (18)$$

By using (18), the output of a double accumulator (left-hand side) can be compared to the output of a single accumulator (right-hand side) to determine the moment to deactivate the auxiliary circuit $t_{\text{aux\_dis}}$, as shown in Fig. 11.

In order to minimize the digital gate count of the controller, it is beneficial to design one double accumulator that can be used for Case #1, Case #2, and cases without load-line regulation. In order to achieve this, charge balance (18) can be modified by multiplying both sides by $(V_{\text{in}} - V_o)$ as

$$(V_{\text{in}} - V_o) \cdot \iint_{t_0}^{t_1} dt\, dt - (V_{\text{in}} - V_o) \cdot \int_{t_{\text{mid}}}^{t_{\text{aux\_dis}}} \left(2 \cdot \int_{t_1}^{t_{\text{mid}}} dt \right) d\tau = R_{\text{droop}} \cdot C_o \cdot (V_{\text{in}} - V_o) \cdot \left(\int_{t_0}^{t_1} dt + 2 \cdot \int_{t_1}^{t_{\text{mid}}} dt \right). \quad (19)$$

By utilizing the combination of (14) and (19), one double accumulator can be used for all cases, as shown in Fig. 12.

Fig. 12 illustrates the load-line accumulator output for Case #2, Case #1, and no load-line (from top to bottom).

The detection of Case #2 will occur between time instants t_{mid} and t_{iL}. As shown, if the output of *accumulator 2* decreases below that of the *load-line accumulator* before t_{iL}, Case #2 is detected and the auxiliary circuit is deactivated at time $t_{\text{aux\_dis}}$. If this condition does not occur, Case #1 is detected. If t_{iL} occurs before the output of *accumulator 2* decreases below the output of

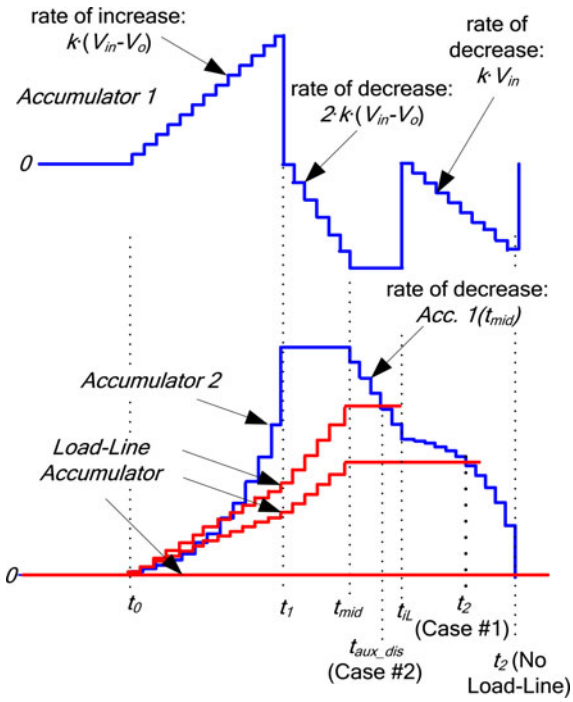

Fig. 12. Digital double accumulator operation for all possible cases.

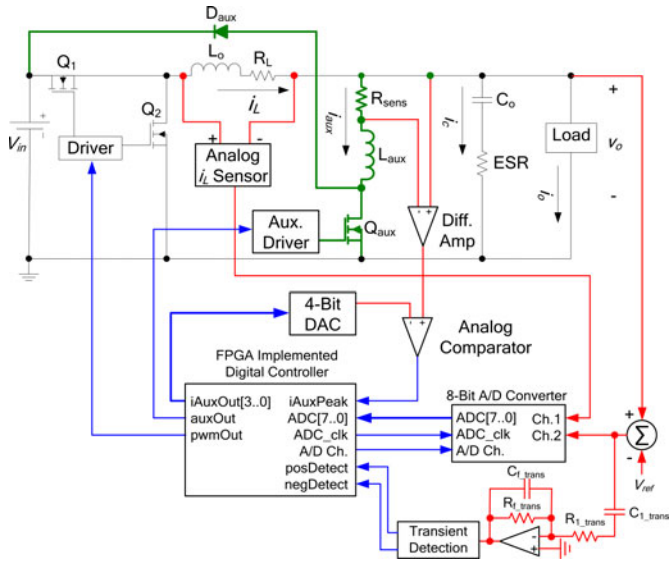

Fig. 13. System-level block diagram of digitally implemented charge balance controller with auxiliary circuit.

the *load-line accumulator*, the auxiliary circuit is deactivated at t_{iL}, as shown in Figs. 4 and 5. In these cases, the buck converter's PWM signal will remain low until output of *accumulator 2* decreases below the *load-line accumulator*'s output at time t_2.

Referring to the final charge balance equations (7), (14), and (19), it is noted that L_o has cancelled out of the equations. Therefore, the knowledge of L_o is not required for proper capacitor charge balance. This is a significant advantage of the proposed control method.

IV. Detailed Operation and Implementation of Charge Balance Controller With Auxiliary Circuit

The high-level system diagram of the digital charge balance controller with auxiliary circuit for a synchronous buck converter is illustrated in Fig. 13. The logic level diagram of the aforementioned double accumulator is shown in Fig. 14.

This section summarizes the operation of the proposed charge balance controller with the auxiliary circuit. The operation of the controller can be summarized in eight steps.

Step 1 ($t = t_0$):

The Buck converter is controlled by a digital linear controller during the steady-state operation. Following an unloading transient, the output of the analog load transient detector (see Fig. 13) will rapidly exceed a predetermined transient threshold. The output of the analog transient detector can be very noisy if it is not designed correctly. However, for this application, the transient detector can be designed such that it does not significantly amplify high-frequency noise.

In previous works, such a circuit was either designed as a pure differentiator or such that the time constant equaled the buck converter's output capacitor (C_o and ESR). A pure differentiator amplifies high-frequency noise to infinity and is practically infeasible. However, even in the latter case, the effective equivalent series resistance (ESR) of most low voltage/high current buck converter applications is so low that the circuit still amplifies high-frequency noise.

In the aforementioned works, the purpose of designing such a fast circuit is to continuously track the capacitor current. Therefore, the transfer function of the circuit must be tuned precisely in order to estimate the capacitor current without delay while ensuring that high-frequency noise does not significantly pollute the output. However, in this paper, the analog transient detector is only used as a means to detect the beginning of a load transient. Therefore, a high-pass filter with a relatively low gain and corner frequency may be used with acceptable results.

In order to attenuate very high frequency noise, a small capacitor can be added in parallel with R_{f_trans}, effectively creating a simple bandpass filter. By increasing C_{f_trans}, better noise immunity can be achieved at the cost of potentially increasing the activation delay.

The activation threshold should be set larger than half the steady-state output voltage ripple, multiplied by $R_{f\_\mathrm{trans}}/R_{1\_\mathrm{trans}}$, to ensure that only load transients trip the threshold. However, it should be noted that if the switching frequency is below the corner frequency of the transient detected, tighter thresholds may be used. When a load transient occurs, the high-frequency output voltage components, caused by the ESR and equivalent series inductance (ESL) of the capacitor, pass through the high-pass filter. This allows for very fast detection of the load transient. The analog-to-digital converter (ADC) may also be used for transient detection at a cost of reaction speed. If the ADC sampling rate and data latency were in an acceptable range, the analog circuitry could be eliminated.

The detection of the load transient will cause the controller to immediately enter transient mode. The linear controller will

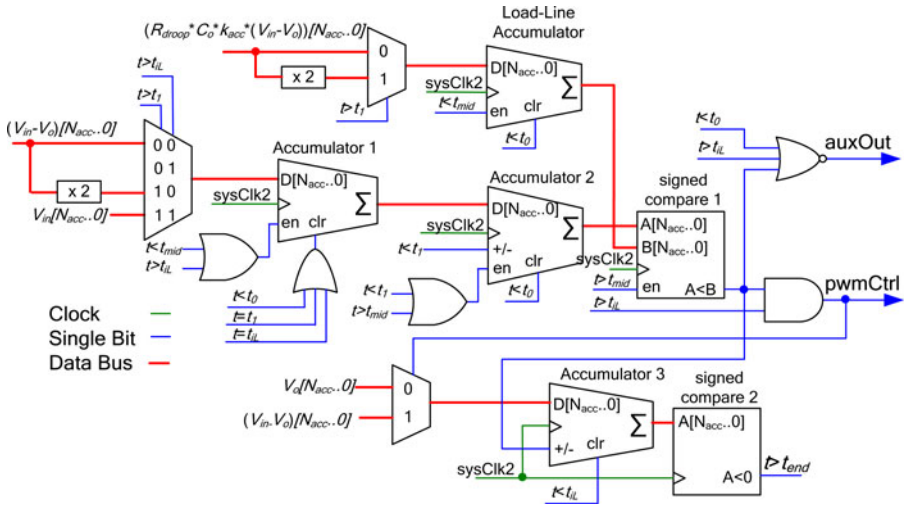

Fig. 14. Logic diagram of double accumulator structure.

be frozen and the charge balance controller will take control of the converter.

The PWM signal of the buck converter will be initially set low and the PWM signal of the auxiliary circuit will be initially set high.

As shown in Fig. 12, the output of *accumulator 1* will begin to increase linearly with a slope of $k \cdot (V_{\rm in} - V_o)$ and the output of *accumulator 2* will begin to increase exponentially. If load-line regulation is required, the *load-line accumulator* will begin to increase linearly with a slope of $k^2 \cdot R_{\rm droop} \cdot C_o \cdot (V_{\rm in} - V_o)$.

It is noted in Fig. 14 that $V_{\rm in}$ is treated as a known constant. As the ratio of $V_o/V_{\rm in}$ increases, the dependence on $V_{\rm in}$ in the charge balance equations increases. It is assumed in the equations that $V_{\rm in}$ is known and constant. If these assumptions are untrue (i.e., $V_{\rm in}$ has a large tolerance or can change significantly), it is recommended that $V_{\rm in}$ be measured by an ADC and be inserted into the system illustrated in Fig. 14 as a variable (as opposed to a constant).

Step 2 ($t_{\rm samp1} \le t \le t_{\rm samp2}$):

As shown in Figs. 4–6, two output voltage samples are acquired at $t_{\rm samp1}$ and $t_{\rm samp2}$ to estimate the load transient magnitude. Using this information and (20), an appropriate value of $I_{\rm aux\_peak}$ is selected from a lookup table (LUT). $I_{\rm aux\_peak}$ is passed to the system's 4-bit digital-to-analog converter (DAC) (see Fig. 13)

$$\Delta I_o = C_o \cdot \frac{v_o(t_{\rm samp2}) - v_o(t_{\rm samp1})}{t_{\rm samp2} - t_{\rm samp1}} + \left[V_o \cdot \left(\frac{1}{L_{\rm aux}} + \frac{1}{L_o}\right) \cdot (t_{\rm samp2} - 1/2 \cdot T_{\rm samp} - t_0) + {\rm ESR}\right]. \quad (20)$$

At $t_{\rm samp2}$, the auxiliary circuit will begin high-frequency switching operation using peak-current constant off-time control.

The LUT allows the user to have design flexibility. The appropriate peak current is user-defined based on the desired output voltage response.

It is noted in (20) that $L_{\rm aux}$ and L_o are required for load current estimation (and subsequently $I_{\rm aux\_peak}$ selection). Therefore, $L_{\rm aux}$ and/or L_o tolerance may result in suboptimal $I_{\rm aux\_peak}$ selection; however, choosing a suboptimal $I_{\rm aux\_peak}$ will not negatively affect the charge balance calculations.

Peak current selection is a tradeoff between transient voltage response and system efficiency/auxiliary circuit sizing. However, in the proposed control method, the relationship between the average auxiliary current and the magnitude of the load step must satisfy the following equation:

$$\Delta I_o \ge 2 I_{\rm aux\_avg}. \quad (21)$$

It is noted that in order to input the appropriate $I_{\rm aux\_peak}$ values, the maximum possible load step should be defined in advance for the system. However, this is a typical requirement for all voltage regulator design.

It is shown in Fig. 13 that an analog comparator is used to detect the peak auxiliary current $I_{\rm aux\_peak}$. The detection signal is used by the digital controller. The mixed-signal implementation is necessary due to the high slew rate of the auxiliary current.

Step 3 ($t = t_1$):

The capacitor current crosses zero for the first time at t_1. In order to predict the time instances t_1, $t_{\rm mid}$, and t_{iL}, a capacitor current zero-crossover predictor is utilized. The predictor acquires output voltage samples (at a frequency equivalent to auxiliary circuit switching frequency $f_{\rm aux}$) for a short period after t_0. From these samples, it is possible to calculate the derivative and estimate the capacitor current slope and magnitude allowing for the fine resolution prediction of t_1, $t_{\rm mid}$, and t_{iL}, as shown in Fig. 15.

In this implementation, three voltage samples were used to estimate the capacitor current slope and predict its zero-crossover point t_1.

The illustrated zero-crossover detection method assumes an ideal capacitor with zero ESR. If the ESR of the output capacitor bank is significant, a constant digital delay (of $T_{\rm del\_ESR} = C_o \cdot {\rm ESR}$) may be added to the detection of t_1, $t_{\rm mid}$, and t_{iL} to

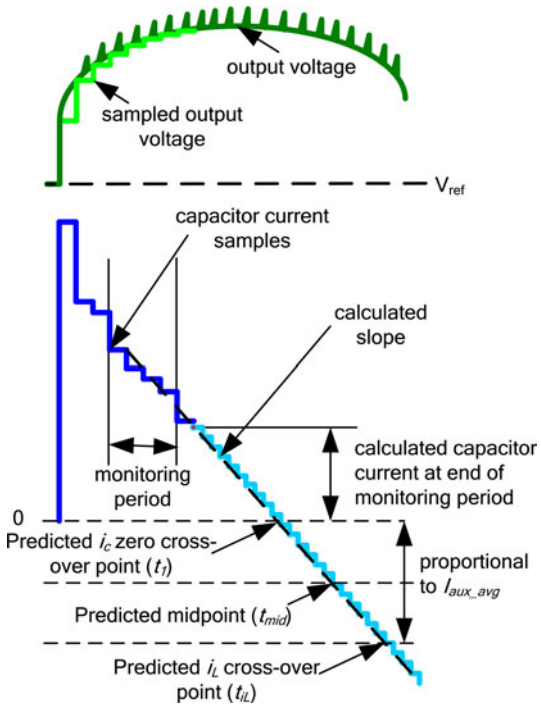

Fig. 15. Prediction of t_1, $t_{\rm mid}$, and t_{iL} by capacitor current zero-crossover predictor.

compensate. In the proposed controller, this was accomplished by using a digital counter.

The detection of $t_{\rm mid}$ and t_{iL} is calculated based on the knowledge of the average auxiliary current $I_{\rm aux\_avg}$. For each peak auxiliary current available through the aforementioned LUT, a corresponding $I_{\rm aux\_avg}$ must also be programmed into the controller. This allows the controller to accurately calculate t_{iL}. It should be noted that there is no assumed relationship between $I_{\rm aux\_peak}$ and $I_{\rm aux\_avg}$. The controller allows for maximum flexibility. For example, if the value of $R_{\rm sens}$ were so large as to significantly alter the relationship between $I_{\rm aux\_peak}$ and $I_{\rm aux\_avg}$, this can easily be reflected in the programmed LUTs.

Referring to Fig. 12, at t_1, *accumulator 1* is reset to zero. The input of *accumulator 1* is set to $-2(V_{\rm in} - V_o)$ and the enable input of *accumulator 2* is set low. Thus, the output of *accumulator 1* will begin to decrease at a rate of $2k(V_{\rm in} - V_o)$ and the output of *accumulator 2* will remain constant.

The channel select of the ADC is set to the inductor current sensor at this point, and a sample of the inductor current is taken and passed to the linear controller. This will be used when load-line regulation is employed to allow for immediate load tracking by the linear controller when it regains control of the system.

Referring to Fig. 12, the input of the *load-line accumulator* is switched to $2k \cdot R_{\rm droop} \cdot C_o \cdot (V_{\rm in} - V_o)$ at t_1.

Step 4 ($t = t_{\rm mid}$):

When the i_c zero-crossover predictor indicates $t = t_{\rm mid}$, it is known that $i_L - I_{o2} = \frac{1}{2} \cdot I_{\rm aux\_avg}$. Referring to Fig. 12, at $t = t_{\rm mid}$, the *enable* input of *accumulator 1* is set low and the enable input of *accumulator 2* is set high. *Accumulator 2* is set to decrement mode, causing its output to decrease at a linear rate equal to $k \cdot Acc1(t_{\rm mid})$ (where $Acc1(t_{\rm mid})$ equals the output of *accumulator 1* at $t = t_{\rm mid}$).

As shown in Fig. 12, the enable input of the *load-line accumulator* is set low at $t_{\rm mid}$, causing its input to remain constant following $t_{\rm mid}$.

Step 5 ($t = t_{\rm aux\_dis}$) (Case #2 only):

As shown in Fig. 12, if the output of *accumulator 2* decreases below that of the *load-line accumulator* before the inductor current equals the new load current (at t_{iL}), then Case #2 is detected. If this occurs, the auxiliary circuit is deactivated at this moment ($t = t_{\rm aux\_dis}$), as shown in Fig. 6. The PWM signal of the buck converter continues to be held low.

Step 6 ($t = t_{iL}$):

When the inductor current equals the new load current for the first time, $t = t_{iL}$.

If Case #2 was previously detected, this moment signifies the end of the load transient and the linear controller retakes control of the buck converter.

If Case #2 was not previously detected, *accumulator 1* is cleared and its input is switched to $-V_{\rm in}$. This causes *accumulator 1*'s output to decrease at a rate of $k \cdot V_{\rm in}$ and the output of *accumulator 2* to decrease at an exponential rate. As shown in Figs. 4 and 5, the auxiliary circuit is deactivated and the PWM control signal is held low following t_{iL}.

Step 7 ($t = t_2$) (No Load-Line Regulation or Case #1):

When the output of *accumulator 2* decreases below that of the *load-line accumulator* (at t_2), the PWM signal of the buck converter is switched high and the inductor current begins to increase toward the new load current, as shown in Figs. 4 and 5.

Step 8 ($t = t_{\rm end}$):

When the inductor current equals the new load current for the first time (for Case #2) or the inductor current equals the new load current for a second time, it is determined that the transient is over. The second current crossover is detected using a digital accumulator (*accumulator 3*), as introduced in [2]. The linear controller is unfrozen and retakes control of the buck converter. If load-line regulation is used, the sampled inductor current (at t_1) is passed to the linear controller for instant load tracking.

V. Simulation Results

The following simulation was conducted under the ideal case, without considering timing delays, digital quantization effects, etc.

All analog sampling/reaction delays were included in the simulation; however, digital calculation delays were not included. The simulations were performed using a primarily analog-centric simulator that was not able to properly model the propagation delays of the field-programmable gate array (FPGA). However, since the system clock of the FPGA was 250 MHz, 4-ns clock delays will have insignificant effects on the charge balance time durations (which are typical three orders of magnitude larger).

The purpose of the simulation was to demonstrate the effectiveness of the charge balance controller with the auxiliary circuit over 1) a linear analog controller and 2) the charge balance controller alone.

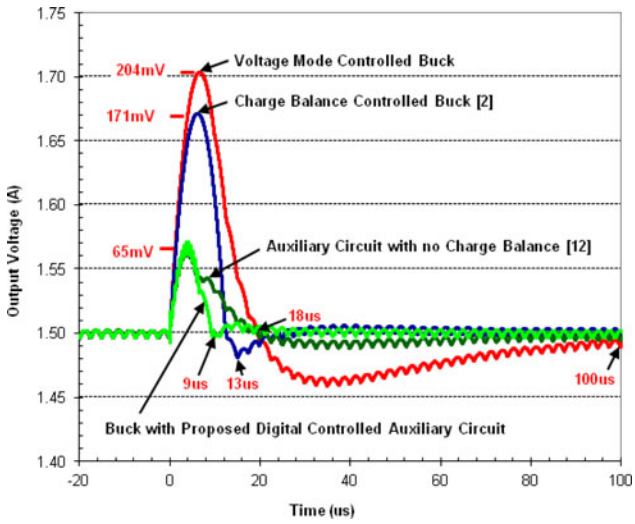

Fig. 16. Simulated response to a 10 A→0 A load current step change without load-line regulation ($I_{\mathrm{aux\_avg}} = 3.8$ A).

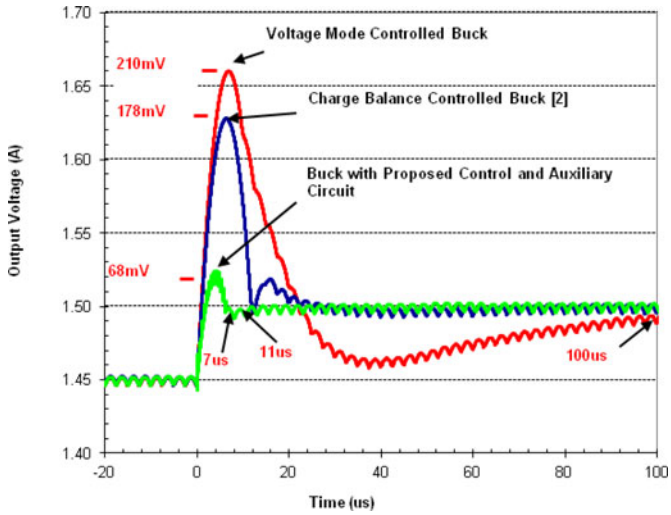

Fig. 17. Simulated response to a 10 A→0 A load current step change with load-line regulation ($I_{\mathrm{aux\_avg}} = 3.8$ A).

The parameters of the simulated buck converter were as follows: $V_{\mathrm{in}} = 12$ V, $V_o = 1.5$ V, $f_{\mathrm{sw}} = 400$ kHz, $L_o = 1$ μH, $L_{o\_\mathrm{DCR}} = 1$ mΩ, $C_o = 180$ μF, ESR $= 0.5$ mΩ, and ESL $=$ 100 pH. The auxiliary circuit parameters were $L_{\mathrm{aux}} = 100$ nH, $L_{\mathrm{aux\_DCR}} = 0.3$ mΩ), and $f_{\mathrm{aux}} \approx 2$ MHz.

Fig. 16 shows the simulated comparison (without load-line regulation) of a voltage-mode controlled converter, a charge balance controlled converter (without auxiliary circuit [2]), a converter with the auxiliary circuit (without charge balance control [12]), and the proposed digital charge balance controller with auxiliary circuit undergoing a 10 A→0 A load step. In this case, the auxiliary circuit sets $I_{\mathrm{aux\_avg}}$ to approximately 3.8 A.

It is illustrated that the voltage deviation magnitude and the settling time is improved significantly over previously proposed solutions. The buck converter with the proposed controller and auxiliary circuit has an output voltage overshoot of 65 mV and a settling time of 9 μs.

The transient response was also simulated with load-line regulation. The output impedance R_{droop} was set to 5 mΩ. Fig. 17 illustrates a simulated comparison between a voltage-mode controlled converter, a digital charge balance controlled buck converter (without auxiliary circuit) [2], and the proposed digital charge balance controller with auxiliary circuit. Each converter undergoes a 10 A→0 A load step transient. The peak auxiliary current is set such that the average auxiliary current equals $I_{\mathrm{aux\_avg}} = 3.8$ A.

It is illustrated that the voltage deviation magnitude and the settling time are improved significantly over previously proposed solutions. The buck converter with the proposed controller and auxiliary circuit has an output voltage overshoot of 18 mV (68–50 mV) over the new steady-state voltage (68 mV over the original steady-state voltage) and a settling time of 7 μs.

VI. Experimental Results

The proposed controller was implemented on an Altera Cyclone II FPGA. The chip is capable of utilizing over 70 000 logic elements; however, the charge balance controller (including the i_c zero-crossover predictor and the double accumulator blocks) only requires a total of approximately 450 logic elements. As a reference point, the digital-type III compensator and digital pulsewidth modulator require 450 logic elements to implement (not including its LUTs). It is important to note that multiplier, divider, square root, or 2-D LUTs are *not* required to implement the digital charge balance controller.

As noted in Fig. 15, the effective sampling frequency should equal the auxiliary switching frequency in order to predict the capacitor current zero-crossover point. If the chosen ADC has a multicycle latency, it may be necessary to use a faster ADC and oversample in order to reduce data latency. The effective data latency must be compensated for in the capacitor zero-crossover algorithm. In the experimental prototype, the ADC latency was 40 ns.

The high-pass filter corner frequency of the analog transient detector was set to approximately 600 kHz, and the gain was set to 5. Therefore, the parameters were $C_{1\_\mathrm{trans}} = 1$ nF, $R_{1\_\mathrm{trans}} =$ 300 Ω, and $R_{f\_\mathrm{trans}} = 1.5$ kΩ. C_{f_trans} was equal to 10 pF. The buck converter and auxiliary circuit parameters were identical to those of the simulation.

Fig. 18 illustrates the controller's reaction to an 11.5 A→0 A load step (without load-line regulation). For this unloading magnitude, the auxiliary current was set to approximately $I_{\mathrm{aux\_avg}} =$ 3.5 A.

It should be noted that the simulation test conditions (load step magnitude and auxiliary current) are slightly different than the experimental prototype test conditions; therefore, the results differ as well. As mentioned, the primary purpose of the simulation was to compare to previous works in order to demonstrate the effective improvement. Thus, the simulation results were chosen to match the conditions of the previous work. For reference, the time instants t_0–t_{end} were superimposed on the scope display to better illustrate the controller's behavior.

The converter is capable of recovering from the load transient within 9 μs with a voltage overshoot of 70 mV.

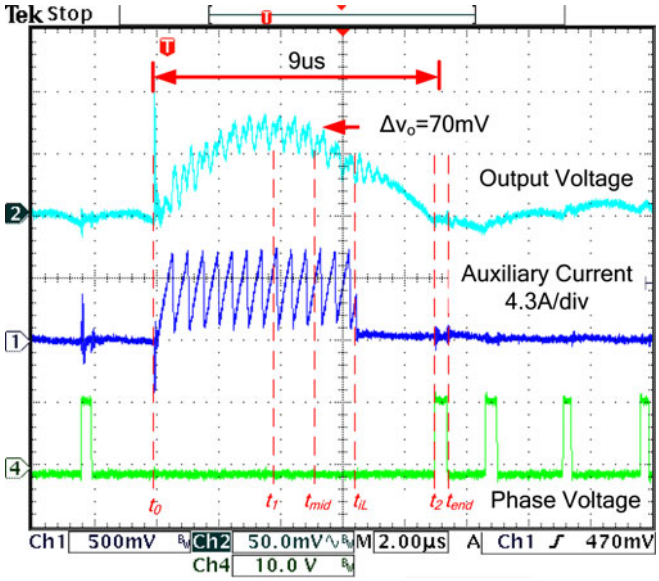

Fig. 18. Digital charge balance controller's response to a 11.5 A→0 A load step without load-line regulation.

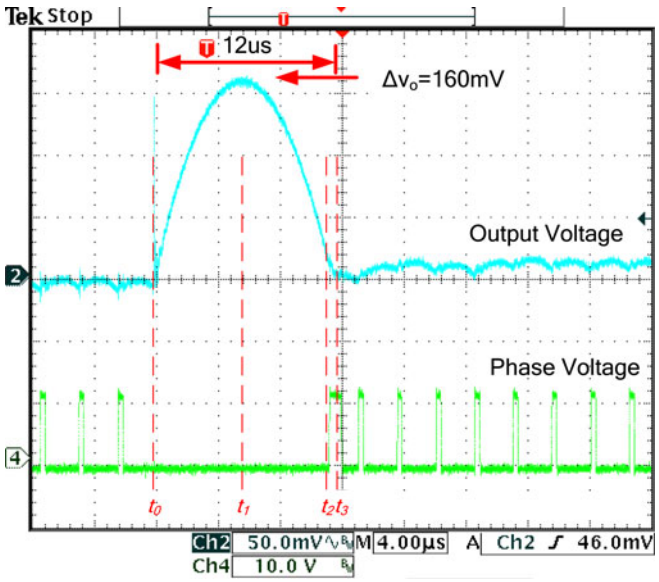

Fig. 19. Digital charge balance controller's response (without auxiliary circuit) to a 11.5 A→0 A load step without load-line regulation.

Fig. 19 illustrates the unloading transient response of the digital charge balance controller (introduced in [2]) without the use of the auxiliary circuit.

As observed, the use of the auxiliary circuit improves the settling time by 25% (12 μs→9 μs) and improves the voltage overshoot by 56% (160 mV→70 mV) over that of the digital charge balance controller alone.

Therefore, if the auxiliary circuit were not utilized and a 70 mV overshoot was still required, the output capacitance would need to be increased to approximately 180 μF × (160 mV/70 mV) = 411 μF (neglecting ESR effects).

Therefore, assuming the output capacitance was made up of ten 0805 size 22-μF ceramic capacitors (with an effective capacitance of 18 μF due to dc bias), an additional 13 capacitors would be required to reduce the overshoot to 70 mV. Thus, an additional area of (13 × 2 mm × 1.3 mm plus an x-direction component to component spacing of 0.4 mm) 42.6 mm^2 would be required.

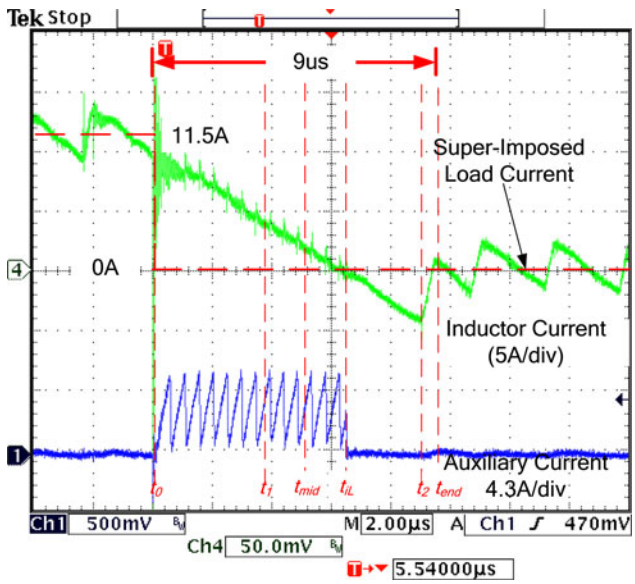

Fig. 20. Digital charge balance controller's response to a 11.5 A→0 A load step without load-line regulation (inductor current and auxiliary current).

To estimate the optimized area of the auxiliary circuitry, the following assumptions are made: 1) the additional auxiliary MOSFET driver can and control circuitry can be integrated in the existing controller, 2) Q_aux and D_aux could be integrated together in a 3 mm × 3 mm QFN package (similar to Infineon's BSZ0907ND), 3) the inductor footprint space is 5.18 mm × 5.49 mm (similar to Vishay Dale's IHLP-2020BZ-01), and 4) a 1206 (3.2 mm × 1.6 mm) resistor could be used for current sensing. Based on these assumptions, the auxiliary circuitry would be approximately 42.5 mm^2. Fig. 20 illustrates the inductor current (measured from the analog inductor current filter) and the auxiliary current. For reference, the load current and time instants t_0–$t_{\rm end}$ were superimposed on the graph.

As shown in Fig. 20, the auxiliary circuit is deactivated when the inductor current first equals the new load current (at t_{iL}). However, the buck converter's PWM signal is kept low until t_2 is determined. This is to allow additional charge to be removed from the output capacitor such that the output voltage equals the reference voltage at the exact moment that the inductor current equals its new steady-state value.

Fig. 21 illustrates the digital signals of the controller during the unloading transient. The digital signals were extracted during experimental tests using an embedded logic analyser. For reference, time instants t_0–$t_{\rm end}$ were superimposed on the graph. Fig. 22 illustrates the controller's reaction to a 17.5 A→0 A load step (without load-line regulation). For this unloading transient magnitude, the auxiliary current was set to approximately $I_{\rm aux\_avg}$ = 8 A. For reference, the time instants t_0–$t_{\rm end}$ were

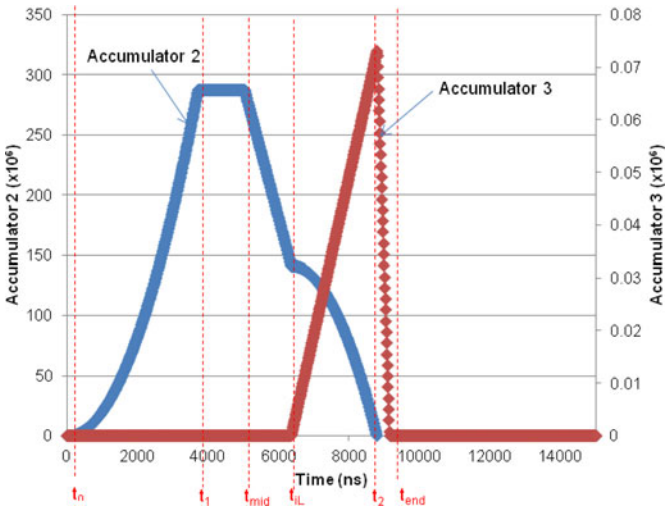

Fig. 21. Digital control signals of charge balance controller during 11.5 A→0 A load current transient without load-line regulation.

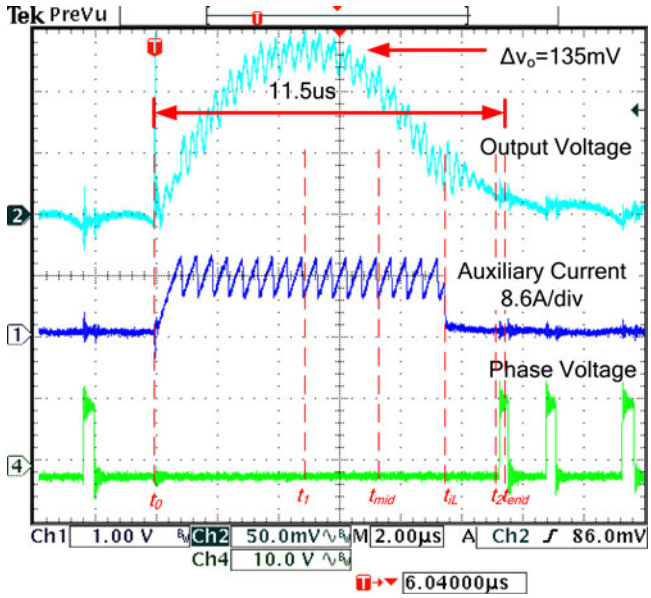

Fig. 22. Digital charge balance controller's response to a 17.5 A→0 A load step without load-line regulation (output voltage, auxiliary current, and phase voltage).

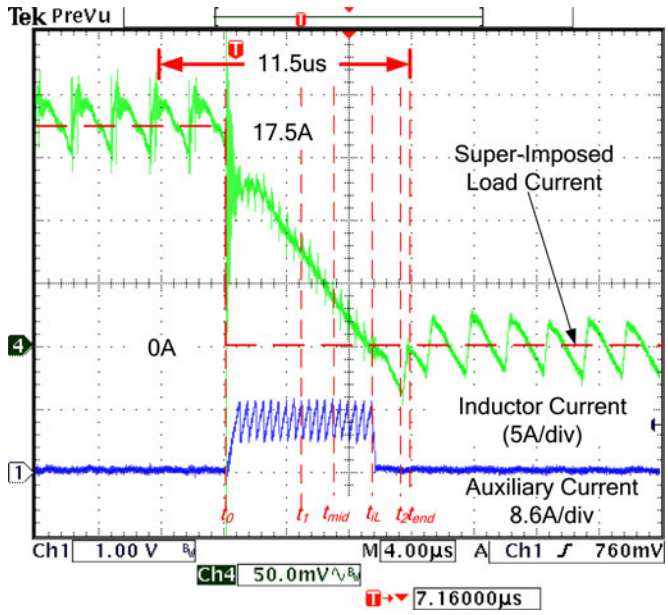

Fig. 23. Digital charge balance controller's response to a 17.5 A→0 A load step without load-line regulation (inductor current and auxiliary current).

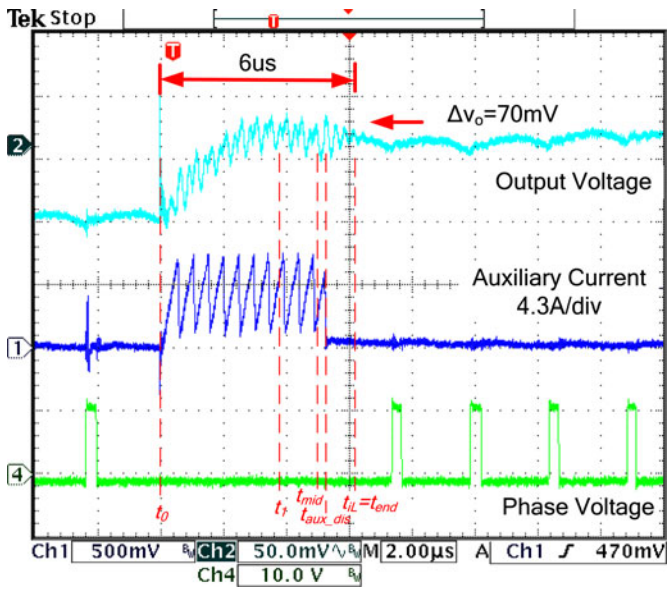

Fig. 24. Digital charge balance controller's response to an 11.5 A→0 A load step with load-line regulation.

superimposed on the scope display to better illustrate the controller's behavior.

As shown, the converter is capable of recovering from the load transient within 11.5 μs with a voltage overshoot of 135 mV.

In order to achieve a 135-mV overshoot without the auxiliary circuit, 750 μF of capacitance would be required. This is based on the following formula (derived from [1]):

$$\Delta v_{o_{\text{neg}}} = \frac{\text{ESR}^2 \cdot C_o^2 \cdot V_o^2 + \Delta I_o^2 \cdot L_o^2}{2 \cdot V_o \cdot L_o \cdot C_o}. \tag{22}$$

Therefore, assuming the output capacitance was made up of ten 0805 size 22-μF ceramic capacitors (with an effective capacitance of 18 μF due to dc bias), an additional 32 capacitors would be required to reduce the overshoot to 135 mV. Thus, an additional area of (32 × 2 mm × 1.3 mm plus an x-direction component to component spacing of 0.4 mm) 107.2 mm^2 would be required. In this case, large C_o capacitors may be employed such as 47-μF ceramic capacitors or aluminum polymer capacitors; however, other factors may need to be considered such as per-unit cost and/or height restrictions.

It is noted that simply adding output capacitance limits the converter's speed to change output voltage set points. The proposed method reduces the voltage overshoot without limiting the converter bandwidth.

Fig. 23 illustrates the inductor current (measured from the analog inductor current filter) and the auxiliary current. For

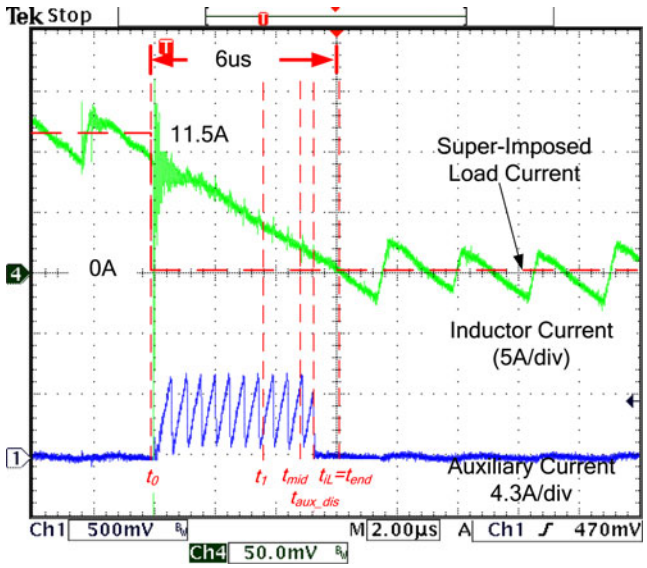

Fig. 25. Digital charge balance controller's response to an 11.5 A→0 A load step with load-line regulation (inductor current and auxiliary current).

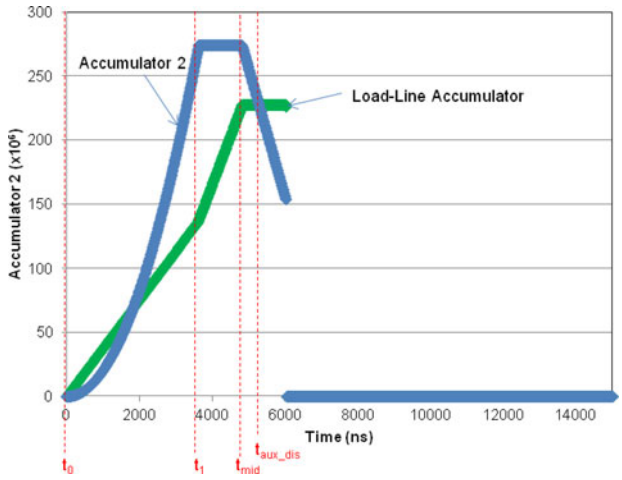

Fig. 26. Digital control signals of charge balance controller during 11.5 A→0 A load current transient with load-line regulation (Case #2).

reference, the load current and time instants t_0–$t_{\rm end}$ were superimposed on the graph. As shown in Figs. 22 and 23, the inductor current returns to the new load current at moment that the output voltage returns to its reference value. Fig. 24 illustrates the controller's reaction to an 11.5 A→0 A load step (with load-line regulation). Fig. 25 illustrates the inductor current (measured from the analog inductor current sensor). Fig. 26 shows the experimentally obtained digital signals of the controller during the negative load current step transient with load-line regulation.

Since the output of *accumulator 2* is less than that of the *load-line accumulator* before t_{iL}, Case #2 is detected and the auxiliary current is deactivated at $t_{\rm aux\_dis}$ to allow the capacitor charge areas to balance by time t_{iL}. This results in a smooth transition as the output voltage equals its new steady-state value at the exact moment that the inductor current equals the new load current. The converter is able to recover from the unloading step within 6 μs and with only a 10 mV (70–60 mV) overshoot beyond the final steady-state voltage.

VII. Conclusion

In this paper, a novel digital charge balance control method is described capable of reducing the voltage overshoot of a buck converter (through the use of an auxiliary circuit) *and* implementing load-line regulation. The proposed digital controller does not require multipliers, dividers, or 2-D LUTs, significantly reducing the IC real-estate required. The proposed control algorithm consumes an additional 450 Altera logic elements over the 450 logic elements required for the steady-state voltage-mode controller.

The use of the auxiliary circuit significantly reduces the voltage overshoot (due to an unloading transient) beyond the physical capabilities of the buck converter alone. It is shown that by implementing the charge balance principle with the auxiliary circuit, the settling time can be also significantly improved over previously proposed solutions. In addition, it is demonstrated that load-line regulation can be implemented while still allowing for a nearly seamless transition between the nonlinear and linear control methods. Extensive experimental results are provided to verify the advantages of the proposed control method.

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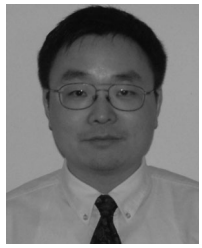

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